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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 34

Application Number: 07/985,141
Filing Date: December 3, 1992
Appellant(s): Katsura et al.

Carl I. Brundidge
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed January 8, 1999.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 44-66 under 35 USC 251 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

Appellant's brief includes a statement that claims 44-57 and 63-66 (as rejected under 35 USC 103) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,716,527	Graciotti	12/1987
4,796,231	Pinkham	1/1989
63-83844	Takenaka	4/1988

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

35 U.S.C. § 251

The supplemental reissue oath or declaration is defective because it fails to particularly specify the errors relied upon, as required under. 37 C.F.R. § 1.175(a)(3) and (5)

37 C.F.R. § 1.175 reads as follows (emphasis added):

§ 1.175 Reissue oath or declaration.

(a) Applicants for reissue, in addition to complying with the requirements of § 1.63, must also file with their applications a statement under oath or declaration as follows:

(1) When the applicant verily believes the original patent to be wholly or partly inoperative or invalid, stating such belief and the reasons why.

(2) When it is claimed that such patent is so inoperative or invalid "by reason of a defective specification or drawing" particularly specifying such defects .

(3) When it is claimed that such patent is inoperative or invalid " by reason of the patentee claiming more or less than he had the right to claim in the patent," distinctly specifying the excess or insufficiency in the claims.

(4) [Reserved]

(5) Particularly specifying the errors relied upon, and how they arose or occurred.

(6) Stating that said errors arose "without any deceptive intention" on the part of the applicant.

(7) Acknowledging the duty to disclose to the Office all information known to applicants to be material to patentability as defined in § 1.56.

(b) Corroborating affidavits or declarations of others may be filed and the examiner may, in any case, require additional information or affidavits or declarations concerning the application for reissue and its object.

Page 3 of the supplemental declaration identifies the error as the appellant's not realizing that the invention could have been claimed more broadly "to more simply recite that the invention provides "a first bus having M lines interconnecting a memory and a memory controller and a second bus having N lines interconnecting data processor and the memory controller, wherein N and M are integers and N is greater than M, and that the memory controller transfers M bits of data to and from the memory in a time shared fashion and transfers N bits of data in parallel to and from the data processor."

Because the present claims are more narrow (conversion means, first and second conversion means, conversion in response to an indication from the processor, storage for temporarily storing graphics data, . . .), the error distinctly specified in the supplemental declaration no longer applies to any of the present claims.

35 U.S.C. § 103

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

Claims 44-58, 63-66 are rejected under 35 U.S.C. § 103 as being unpatentable over Graciotti (4,716,527) in view of Takenaka (63-83844) and Pinkham (4,796,231).

a. As per independent claims 44, 49, 57 and 63, Graciotti discloses at column 3, lines 1-50 a system which converts data to make an m byte wide data

bus compatible with an n byte wide data bus (where n > m) by arranging or extracting upper and lower portions. Graciotti discloses at column 3, lines 9-11 and 48-50 that the operation is bidirectional. Graciotti further discloses at column 5, line 34 through column 6, line 36 that means are provided for selecting the lower byte and higher byte. Graciotti shows in figure 1 that storage means (31, 38 and 39) are provided for temporarily storing data. Graciotti further discloses at column 3, lines 61 through column 4, line 5 that the conversion is in response to signals from the microprocessor.

Regarding the language in claim 63 directed to "terminals", Graciotti discloses an integrated circuit implementation of a circuit interfacing two data buses. The examiner takes official notice that it was known in the art at the time the invention was made that integrated circuits included terminals for physically connecting the circuit to data lines, address lines and signal lines.

It is noted that Graciotti does not explicitly disclose that graphics data is processed, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Graciotti as claimed because Graciotti discloses a bus conversion system for general purpose use including Input/output devices (column 2, line 48) and floppy disk controllers (column 2, lines 13-33) and such devices are often used to process graphics data. For

example, it is well known in the art that input devices such as scanners and output devices such as crt displays require a memory for storing graphics data. It is also well known that graphics data can be stored in files which in turn can be stored on floppy disks. Since Graciotti does not limit the disclosed invention to any one type of data, it would have been obvious to one of ordinary skill in the art at the time the invention was made to used the conversion system disclosed by Graciotti for graphics data because this is suggested by Graciotti's disclosure at column 2, line 48 that the invention may be used for input/output devices.

It is also noted that Graciotti does not explicitly disclose that retrieval is within "a predetermined period of time", however, this is known in the art as disclosed by Takenaka. Takenaka discloses a bus interface similar to Graciotti's and further discloses that the time required to the processor to access the ROM 11 is a predetermined period of time equal to two times the access time of the ROM. It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure Graciotti as claimed because it is well known in the art that computer systems usually define a predetermined time for accessing memory (memory access time) and Graciotti teaches that the conversion is to be transparent, therefore it would have been obvious to maintain the predefined memory access time of the processor as claimed.

It is also noted that Graciotti does not explicitly disclose the claimed conversion means, however, this is known in the art as taught by Pinkham. Pinkham shows in figure 1 a memory access controller which includes storage means (34, 36, 38, 40 and 66) and means for converting the stored data into serial data for output to a display. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Pinkham into the system because, as noted above, Graciotti suggests use in a display system (output devices discussed at column 2, lines 45-49) and Pinkham discloses that memory for displays usually requires conversion of data into serial form (column 1, lines 13-14, 25-47).

b. As per dependent claims 46-48, 50-56, 58, 64 and 65, both Graciotti and Takenaka disclose a system which changes a single 16-bit memory access into two 8-bit memory accesses within a predetermined time (the time for the two 8-bit memory accesses. It is inherent that each memory access required an address signal so that the correct memory location can be accessed.

c. As per dependent claim 66, Graciotti discloses that each m (8) bit portion is either the upper or lower portion of the n (16) bit data.

d. As per dependent claim 45, it is noted that Graciotti does not explicitly disclose a multiplexor, however, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to include this feature because Graciotti does disclose a system which selects between two portions of a word and multiplexors are often used to perform such selections.

e. As per claims 57-58, in addition to the rationale provided above, Pinkham also discloses the use of row and column addressing. See Figure 1, Row address latch 20, Column address latch 22, Row decode 28, and Column select 30.

(11) Response to Argument

35 U.S.C. § 251

Appellant appears to misinterpret 37 CFR § 1.175. Appellant appears to believe that specifying that claiming the patent is inoperative or invalid " by reason of the patentee claiming more or less than he had the right to claim in the patent" is the only requirement (37 CFR 1.175(a)(1). It is clear from 37 CFR § 1.175(a)(3) and (5) that there is an additional requirement. Appellant must also distinctly specify the excess or insufficiency in the claims. This requirement is further explained in MPEP 1414.01 and 1414.03. It is this requirement that is the basis for the rejection.

As noted in the rejection, page 3 of the supplemental reissue declaration specifies the breadth of claim that applicant indicate they have a right to. However, none of the present claims are as broad as what applicant identifies as the breadth required to correct the error. The reissue declaration fails to distinctly specify the excess or insufficiency in the claims,

because the error in the patent is identified as not including claims as broad and that identified at page three of the declaration and the present claims also are not as broad as that identified in the declaration,

The examiner agrees with appellant's statements that the present claims are broader than the patented claims in that they do not require a data processing means (claim 63) or memory that includes an array of location arranged in rows and columns (claim 44), however, they are not as broad as required to correct the error as distinctly specified in the declaration. Had the error been identified as the patented claims including a data processing means that was not required for patentability, this would have been sufficient.

35 U.S.C. § 103

A. GENERAL ARGUMENTS REGARDING ALL CLAIMS.

For this portion of the Appeal Brief, appellant does not identify any specific claims to which these arguments apply. The examiner assumes that appellant intends for these arguments to apply of all of the independent claims that were rejected under 35 U.S.C. § 103 (Claims 44, 49, 57 and 63)

A.1. Memory Controller

Appellant argues that the present claims are directed to a memory controller while Graciotti is directed to a floppy disc controller (Pages 8-9 of the Appeal

Brief). It is the examiner's position that Graciotti is not limited to floppy disc controllers but also discloses used on the controller with memory. Even if Graciotti were limited to floppy disc controllers, a floppy disc is a type of memory and that a floppy disc controller is a type of memory controller.

A.1.i. Graciotti is not limited to floppy disc controllers.

Appellant refers to column 2, lines 9-14 of Graciotti as evidence that Graciotti is limited to floppy disc controllers. Reading further down the column shows that Graciotti does not intend the language "for example, a floppy disc controller" (column 2, line 13) to be limited to the only embodiment. At column 2, lines 45-50, Graciotti refers to "devices such as peripherals, memory expansion or other input/output devices". This clearly indicated that Graciotti's disclosed controller may be used as a memory controller for memory expansion.

A.1.ii. Present claims do not exclude use of a floppy disc controller

Even if Graciotti were limited to floppy disc controllers, the broad language of the claims does not exclude the use of a floppy disc as the claimed memory. The pertinent claim language reads as follows:

"a memory for storing graphic data" (claim 44, line 2)

"a memory means for storing graphic data" (claim 49, line 2)

" A memory controller for controlling transference of data between a memory and a processor" (claim 63, lines 1-3)

There is no limitation in these claims that would exclude the use of a floppy disc as the memory used by the invention. While the specification may not disclose a floppy disc controller and although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

A.2. Successive retrieval of m bits in a predetermined period of time.

Appellant argues that Graciotti does not perform the successive retrievals within a single memory read or write cycle (Pages 8-9 of the Appeal Brief). It is the examiner's position that the rejected claims are not limited to a single read or write cycle. Also, the examiner relies on Takenaka for showing successive retrieval in a predetermined period of time (twice the access time of the ROM11). See the rejection above.

Regarding whether the claims are limited to a single memory read or write cycle, the pertinent claim language appears below:

"a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time" (claim 44, lines 18-20).

The present claims clearly do not require that the predetermined period of time must be limited to a single read or write access time. While this may be disclosed in the specification, and although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The examiner relies on Takenaka for showing successive retrieval in a predetermined period of time (twice the access time of the ROM11). See the rejection above. Appellant has not addressed the application of Takenaka with respect to this limitation.

A.3. Converter

Appellant argues that neither Graciotti or Takenaka suggest a converter within a memory controller (Pages 10-12 and 13 or Appeal Brief). Applicant does admit that Pinkham discloses a converter but questions whether it would have been obvious to incorporate the teaching of Pinkham into Graciotti's system. It is the examiner's position that the claimed converter is suggested by Pinkham for the reasons given in the rejection above and further explained below.

Pinkham shows in figure 1 a memory access controller which includes storage means (34, 36, 38, 40 and 66) and means for converting the stored data into serial data for output to a display. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Pinkham into the system because, as noted above, Graciotti suggests use of the controller in a display system (output devices discussed at column 2, lines 45-49) and Pinkham discloses that display memories usually require conversion of data into serial form (column 1, lines 13-14, 25-47).

Appellant further argues at page 13 of the Appeal Brief that the references do not disclose "the circuits 2019-2025 included in the memory controller 20 . . . wherein graphic data temporarily stored in storage 2015 is converted into serial data which is provided to output means CPLT 40". This specific structure is not

found in the claims. For example, the pertinent portion of claim 44 reads as follows:

"A converter for converting said graphic data temporarily stored in said storage into serial data which is provided to said output means based on an indication from said data processor." (Claim 44, lines 25-28)

As can be seen from the claim language, the present invention does not include circuits 2019-2025 or CPLT 40. It remains the examiner's position that the combination of references applied suggest the claimed converter means.

A.4. Whether the references are combinable

Appellant argues that Graciotti and Pinkham are not combinable because they have different connections and purposes. It is the examiner's position that the connections are not so incompatible that the references do not suggest the present invention. Also, the purposes of Graciotti and Pinkham are very similar.

A.4.i. Connections

In response to appellant arguments that the connections in Graciotti and Pinkham are not compatible, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the

primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

As noted above, Graciotti suggests use of the controller in a display system (output devices discussed at column 2, lines 45-49) and Pinkham discloses that display memories usually require conversion of data into serial form (column 1, lines 13-14, 25-47). This would have suggested to one of ordinary skill in the art at the time the invention was made that when the output device disclosed by Graciotti is a display, a converter should be included so that the output is compatible with to output device and Pinkham indicated that the data should be converted to serial format.

In addition, Appellant fails to explain why the connections should be considered incompatible.

A.4.ii. Purposes

The examiner does not agree that the purposes of Graciotti and Pinkham are different. As noted above, both are directed to accessing data from memory and providing that data to an output device in a format required by the output

device. Appellant fails to explain why the purpose of accessing data as taught by Graciotti is incompatible with the purpose of accessing data as taught by Pinkham.

A.5. Hindsight, "unsupported allegations" and "fabrications"

Appellant accuses the examiner of relying on improper hindsight, "unsupported allegations" and "fabrications" in formulating the rejection. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The only example of alleged improper hindsight, "unsupported allegations" and "fabrications" provided by appellant is that they do not believe it would have been obvious to combine the teachings of Graciotti and Pinkham. As noted in the rejection and section A.4.i. above, Graciotti suggests using the controller in a

display system (output devices discussed at column 2, lines 45-49) and Pinkham discloses that display memories usually require conversion of data into serial form (column 1, lines 13-14, 25-47). It is not clear to the examiner how specific references to column and line numbers within the references can be characterized as improper hindsight, "unsupported allegations" or "fabrications".

B. ARGUMENT DIRECTED TO SPECIFIC CLAIMS

Prior to addressing appellant's specific arguments, the examiner will provide a summary of appellant's arguments and the examiner's position. The appellant makes the repeated allegation that the examiner has not address certain limitations at any point in the prosecution of the application. This is a mischaracterization of the prosecution history. The examiner has repeatedly addressed the argued limitations and pointed to specific teachings in the references to support the rejection. While appellant may disagree with the examiner's position, it is inaccurate to say that the limitations were not addressed. Where necessary, the examiner has clarified his position below.

Dependent Claim 45. Appellant argues that the references do not disclose the claimed multiplexer. The examiner has explained in the rejection above and in previous office actions why this feature would have been obvious based upon the

teachings in Graciotti. Appellant fails to address the basis of the rejection by explain the error in the examiner's rationale.

Dependent claim 46. Appellant argues that the examiner has not address the limitation of generating an address signal for accessing the memory plural times. As noted in the rejection, the references teach that the memory is accessed multiple times. It is inherent in the system that memory addresses be generated in order to access the correct memory locations.

Dependent claim 47. Appellant argues that the examiner has not addressed the limitation that the data is read out from said memory plural times within a unit transfer time in a time shared fashion. As noted in the rejection, both Graciotti and Takenaka disclose a system which changes a single 16-bit memory access into two 8-bit memory accesses within a predetermined time (the time for the two 8-bit memory accesses. In this case, the claimed unit time would equal the time required for the two 8-bit memory accesses. In addition, because there is only one 8-bit bus, the two 8-bit accesses must be performed in a time shared fashion.

Dependent claim 48, Appellant argues that the examiner has not addressed the limitation that the time is longer that twice the unit transfer time. As noted in the rejection, the prior art does suggest multiple memory accessed on the smaller bus. The results of each access are also stored in the temporary memory.

Therefore, the time required in the system suggested by the prior art would include the two accesses to the memory plus the additional access to the temporary memory for a total of three accesses. The three accesses clearly require more time than two accesses as claimed.

Dependent claim 50. This claim is directed to the same limitations as in claim 45 and is rejected under the same rationale. See discussion of claim 45 above.

Dependent claim 51, This claim is directed to the same limitations as in claim 46 and is rejected under the same rationale. See discussion of claim 46 above.

Dependent claim 52, This claim is directed to the same limitations as in claims 46 and 51 and is rejected under the same rationale. See discussion of claim 46 above.

Dependent claim 53, This claim is directed to the same limitations as in claim 47 and is rejected under the same rationale. See discussion of claim 47 above.

Dependent claim 54, This claim is directed to the same limitations as in claim 47 and 53 and is rejected under the same rationale. See discussion of claim 47 above.

Dependent claim 55. This claim is directed to the same limitations as in claim 48 and is rejected under the same rationale. See discussion of claim 48 above.

Dependent claim 56. This claim is directed to the same limitations as in claims 48 and 55 and is rejected under the same rationale. See discussion of claim 48 above.

Dependent claim 58. Appellant argues that the examiner has not addressed the claimed limitation that Pinkham also discloses the use of column addressing. See Figure 1, Row address latch 20, Column address latch 22, Row decode 28, and Column select 30. Appellant fails to explain why this does not suggest the claimed limitation.

Dependent claim 64, Appellant argues that the prior art does not disclose "performing plural read operations within a memory cycle based on an address specified by said processor". This language can be interpreted two ways. In the first interpretation, each of the plural read operations are performed within a memory cycle. This is clearly taught by Graciotti and Takenaka as applied in the rejection. In the second interpretation, from the memory's point of view, there may be multiple memory cycles, from the processors point of view, there is only one cycle (that includes the multiple memory cycles from the memory's point of

view). This second interpretation is consistent with the disclosed invention and corresponds to the system suggested by the prior art.

Dependent claim 65. This claim is directed to the same limitations as in claim 48 and is rejected under the same rationale. See discussion of claim 48 above.

Dependent claim 66. Appellant argues that the examiner has not addressed the limitation that successive groups of m bits of data include am m bit portion of the n bits of data. As was noted in the rejection, Graciotti discloses that each m (8) bit portion is either the upper or lower portion of the n (16) bit data. Appellant fails to address the teachings clearly identified in the previous office actions and repeated in the rejection above.

Independent claim 44, Appellant argues that the examiner has not addressed the limitation that the n bit data is formed using successive groups of m bits of data and providing the n bits in parallel to the processor. Appellant fails to address the examiner's explanation provided in the rejections. As noted above, Graciotti discloses at column 3, lines 1-50 a system which converts data to make an m byte wide data bus compatible with an n byte wide data bus (where $n > m$) by arranging or extracting upper and lower portions. Graciotti discloses at column 3, lines 9-11 and 48-50 that the operation is bidirectional. Where data is

transferred from the m bit bus to the n bit bus it is clear that the n bits are formed from successive m bit data and the n bit data is transferred in parallel (over n bit data bus).

Independent claim 49. Appellant argues that the prior art does not disclose providing the n bit data in parallel to the processor based on an indication from the processor. Any one of ordinary skill in the art at the time of the invention would have recognized that data on an n bit data bus is provided in parallel. And Graciotti discloses a memory controller that performs memory access operations "based on indications from the processor". See for example column 3, line 61 through column 4, line 5 where Graciotti discloses a Memory read signal (AMWR) which is one of the signals provided by the processor that can activate the bus converter. Graciotti further discloses at column 51-60 a signal 16BCH that enables the 16 bit bus mode. It is clear from the teachings of Graciotti that the argued limitation is taught by the applied references.

Independent claim 57. Appellant again argues that the examiner has not addressed the limitations regarding row and column addressing. As was noted in the rejection above and in previous office actions, this feature was specifically addressed in part e of the 103 rejection. Again, appellant fails to address the rationale provided by the examiner.

"The above independent claim" (The examiner assumes appellant means Independent claim 57). Appellant argues that the examiner has failed to address a major portion of the claim limitations. The rationale for the rejection of claim 57 is found in the combination of parts a and e in the rejection above and in previous office actions. Each of the argued limitations have been discussed extensively above. In addition, it should be noted that the term "terminals" does not appear in claim 57. If applicant is referring to claim 63, this limitations has be addressed in the rejection above and in previous office actions.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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